REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21												
REV STATUS OF SHEETS	REV																		
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14				

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
96-08-09

REVISION LEVEL

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, HYBRID, MEMORY, DIGITAL, 512K x 32-BIT, STATIC RANDOM ACCESS MEMORY, CMOS

SIZE	CAGE CODE	
A	**67268**	**5962-95624**

SHEET 1 OF 21

DESC FORM 193
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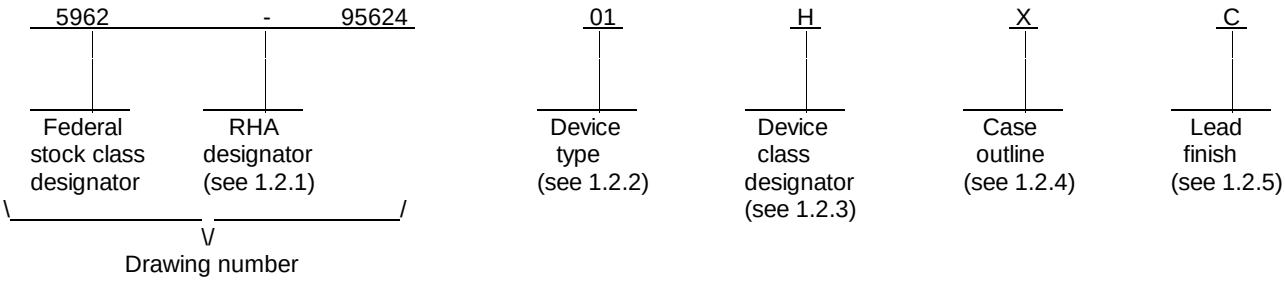
5962-E506-96

1. SCOPE

1.1 Scope. This drawing documents two product assurance classes, high reliability (device class H) and space application (device class K) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes H and K RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	WS512K32F-120G4Q	SRAM, 512K X 32-bit	120 ns
02	WS512K32F-100G4Q	SRAM, 512K X 32-bit	100 ns
03	WS512K32F-85G4Q	SRAM, 512K X 32-bit	85 ns
04	WS512K32F-70G4Q	SRAM, 512K X 32-bit	70 ns
05	WS512K32F-55G4Q	SRAM, 512K X 32-bit	55 ns
06	WS512K32F-45G4Q	SRAM, 512K X 32-bit	45 ns
07	WS512K32F-35G4Q	SRAM, 512K X 32-bit	35 ns
08	WS512K32F-25G4Q	SRAM, 512K X 32-bit	25 ns
09	WS512K32F-20G4Q	SRAM, 512K X 32-bit	20 ns
10	WS512K32M-45G4Q	SRAM, 512K X 32-bit	45 ns
11	WS512K32M-35G4Q	SRAM, 512K X 32-bit	35 ns
12	WS512K32M-25G4Q	SRAM, 512K X 32-bit	25 ns

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device performance documentation
H or K	Certification and qualification to MIL-PRF-38534

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
N	See figure 1	68	Co-fired, single cavity, quad flat pack, low capacitance

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534 for classes H and K.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Signal voltage range (V_G)	-0.5 V dc to +7.0 V dc
Power dissipation (P_D) :	
Device types 01 through 09	2.9 W Max. at 5 MHz
Device types 10 through 12	4.4 W Max. at 5 MHz
Storage temperature range	-65° C to +150° C
Lead temperature (soldering, 10 seconds)	+300° C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input low voltage range (V_{IL})	-0.5 V dc to +0.8 V dc
Input high voltage range (V_{IH})	+2.2 V dc to V_{CC} + 0.3 V dc
Case operating temperature range (T_C)	-55° C to +125° C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbook. The following specification, standards, and handbook form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes H and K shall be in accordance with MIL-PRF-38534 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Timing diagram(s). The timing diagram(s) shall be as specified on figure 4 and 5.

3.2.5 Block diagram(s). The block diagrams shall be as specified on figure 6.

3.2.6 Output load circuit. The output load circuit shall be as specified on figure 7.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of Device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked as listed in QML-38534.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. .

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DC parameters							
Input leakage current	I_{LI}	V_{CC} = 5.5 V dc, V_{IN} = GND or V_{CC}	1,2,3	All		10	μA
Output leakage current	I_{LO}	$\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$, V_{OUT} =GND or V_{CC}	1,2,3	All		10	μA
Operating supply current	I_{CC}	$\overline{CS} = V_{IL}$, $\overline{OE} = V_{IH}$, f = 5MHz, V_{CC} = 5.5 V dc	1,2,3	01-04 05-09 10-12		200 520 800	mA
Standby current	I_{SB}	$\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$, f = 5MHz, V_{CC} = 5.5 V dc	1,2,3	01-04 05-09 10-12		4.0 60 120	mA
Input low level	V_{IL}		1,2,3	All		0.8	V
Input high level	V_{IH}		1,2,3	All	2.2		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 2.1 mA	1,2,3	01-06		0.4	V
		V_{CC} = 4.5 V, I_{OL} = 8.0 mA	1,2,3	07-12		0.4	V
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OL} = -1.0 mA	1,2,3	01-06	2.4		V
		V_{CC} = 4.5 V, I_{OL} = -4.0 mA	1,2,3	07-12	2.4		V
Dynamic characteristics							
$\overline{OE}$ capacitance 3/	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz T_A = +25° C	4	All		32	pF
$\overline{WE}$ capacitance 3/	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz T_A = +25° C	4	All		32	pF
$\overline{CS}_{1-4}$ capacitance 3/	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz T_A = +25° C	4	All		15	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic characteristics- Continued.							
Data I/O capacitance 3/	$C_{I/O}$	V_{IN} = 0 V, f = 1.0 MHz T_A = +25° C	4	All		15	pF
Address input capacitance 3/	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz T_A = +25° C	4	All		32	pF
Functional testing							
Functional tests		See 4.3.1c	7,8A,8B	All			
Data retention characteristics							
Data retention supply voltage	V_{DR}	$\overline{CS} \ge V_{DR}$ - 0.2 V	9,10,11	All	2.0	5.5	V
Data retention current	I_{CCDR1}	V_{CC} = 3 V	9,10,11	01-04 05-09 10-12		1.6 12 40	mA
Read cycle AC timing characteristics							
Read cycle time	t_{RC}	See figure 4	9,10,11	01 02 03 04 05 06,10 07,11 08,12 09	120 100 85 70 55 45 35 25 20		ns
Address access time	t_{AA}	See figure 4	9,10,11	01 02 03 04 05 06,10 07,11 08,12 09		120 100 85 70 55 45 35 25 20	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read cycle AC timing characteristics - Continued.							
Chip select access time	t_{ACS}	See figure 4	9,10,11	01 02 03 04 05 06,10 07,11 08,12 09		120 100 85 70 55 45 35 25 20	ns
Output enable to output valid	t_{OE}	See figure 4	9,10,11	01 02 03 04,10 05-07,11 08,12 09		60 50 40 35 25 12 10	ns
Output hold from address change	t_{OH}	See figure 4	9,10,11	01-04 10-12 05-09	5 5 0		ns
Write AC timing characteristics $\overline{WE}$ controlled .							
Write Cycle time	t_{WC}	See figure 5	9,10,11	01 02 03 04 05 06,10 07,11 08,12 09	120 100 85 70 55 45 35 25 20		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write AC timing characteristics $\overline{WE}$ controlled - Continued.							
Chip select to end of write	t_{CW}	See figure 5	9,10,11	01 02 03 04 05 06,10 07,11 08,12 09	100 80 75 60 50 35 25 17 15		ns
Address valid to end of write	t_{AW}	See figure 5	9,10,11	01 02 03 04 05 06,10 07,11 08,12 09	100 80 75 60 50 35 25 17 15		ns
Data valid to end of write	t_{DW}	See figure 5	9,10,11	01,02 03-04,10 05,06 07,11 08 09 12	40 30 25 20 13 12 10		ns
Write pulse width	t_{WP}	See figure 5	9,10,11	01,02 03,04 05 06,10 07,11 08,12 09	60 50 40 35 25 17 15		ns
Address setup time	t_{AS}	See figure 5	9,10,11	01-04 05-09 10-12	0 2 0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write AC timing characteristics $\overline{WE}$ controlled - Continued.							
Address hold time	t_{AH}	See figure 5	9,10,11	01-06 07-12	5 0		ns
Data hold time	t_{DH}	See figure 5	9,10,11	All	0		ns
Write AC timing characteristics $\overline{CS}$ controlled.							
Write Cycle time	t_{WC}	See figure 5	9,10,11	01 02 03 04 05 06,10 07,11 08,12 09	120 100 85 70 55 45 35 25 20		ns
Chip select to end of write	t_{CW}	See figure 5	9,10,11	01 02 03 04 05 06,10 07,11 08,12 09	100 80 75 60 50 35 25 17 15		ns
Address valid to end of write	t_{AW}	See figure 5	9,10,11	01 02 03 04 05 06,10 07,11 08,12 09	100 80 75 60 50 35 25 17 15		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write AC timing characteristics $\overline{CS}$ controlled - Continued.							
Data valid to end of write	t_{DW}	See figure 5	9,10,11	01,02 03-04,10 05,06 07,11 08 09 12	40 30 25 20 13 12 10		ns
Write pulse width	t_{WP}	See figure 5	9,10,11	01,02 03,04 05 06,10 07,11 08,12 09	60 50 40 35 25 17 15		ns
Address setup time	t_{AS}	See figure 5	9,10,11	01-04 05-09 10-12	0 2 0		ns
Address hold time	t_{AH}	See figure 5	9,10,11	01-06 07-12	5 0		ns
Data hold time	t_{DH}	See figure 5	9,10,11	All	0		ns

1/ Unless otherwise specified, 4.5 V dc $\le V_{CC} \ge$ 5.5 V dc and V_{SS} = 0 V.
2/ Unless otherwise specified, the DC test conditions are as follows:
Input Pulse levels: $V_{IH} = V_{CC}$ - 0.3 V and V_{IL} = 0.3 V.
Unless otherwise specified, the AC test conditions are as follows:
Input Pulse levels: V_{IL} = 0 V and V_{IH} = 3.0 V.
Input rise and fall times: 5 nanoseconds.
Input and output timing reference levels: 1.5 V.
3/ Gurauranteed by design, but not tested.

Case outline N.

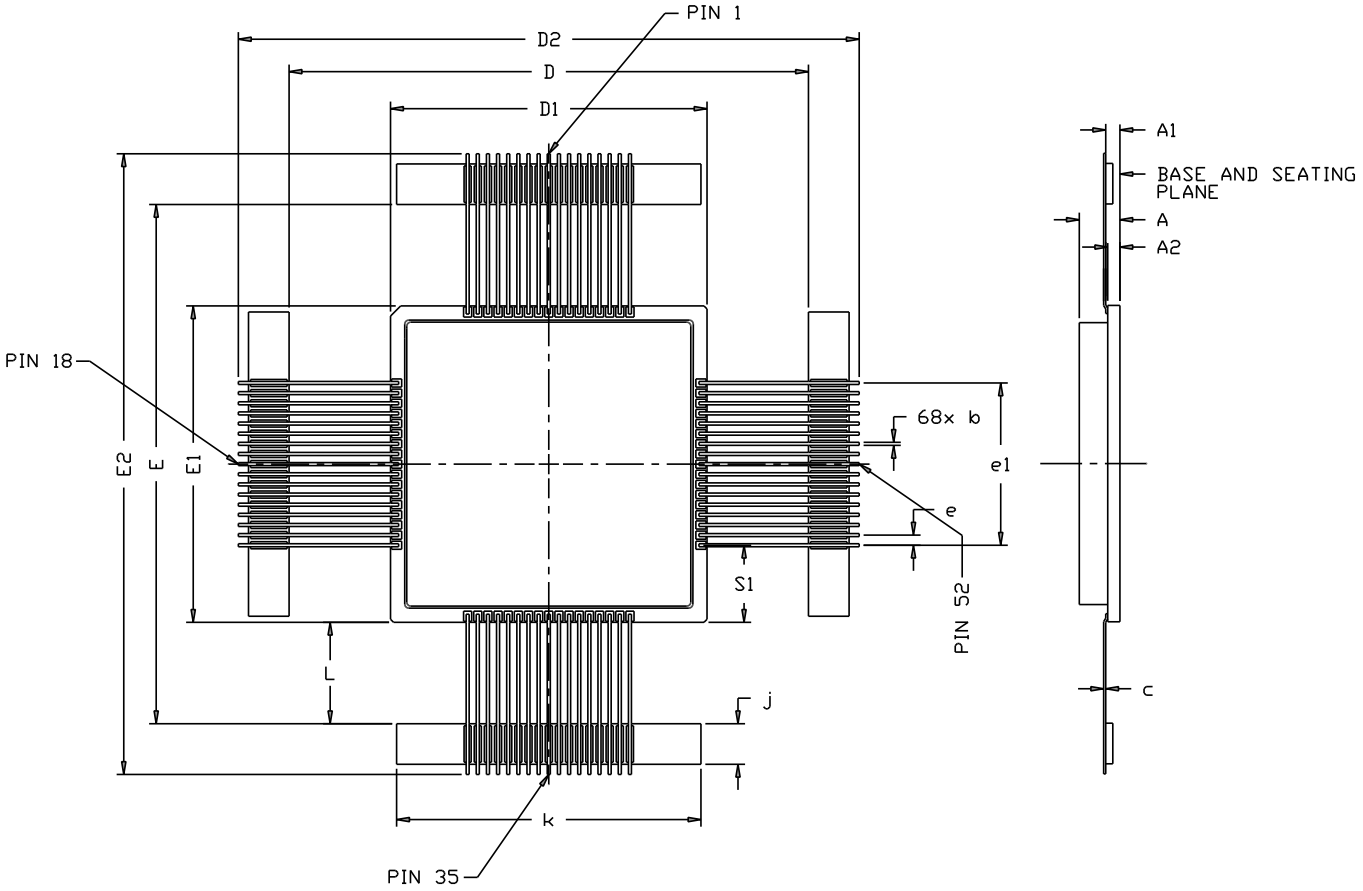


FIGURE 1. Case outlines(s) .

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE **A**		**5962-95624**
		REVISION LEVEL	SHEET **11**

Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.46	5.10	0.175	0.200
A1	1.40	1.65	0.055	0.065
A2	1.14	1.40	0.045	0.055
b	0.30	0.46	0.012	0.018
C	0.23	0.31	0.009	0.012
D/E	63.63	66.42	2.505	2.615
D1/E1	39.24	40.01	1.545	1.575
D2/E2	71.25	84.20	2.805	3.315
e	1.14	1.40	0.045	0.055
e1	20.19	20.45	0.795	0.805
j	4.83	5.33	0.190	0.210
k	37.72	38.48	1.485	1.515
L	12.19	13.21	0.480	0.520
S1	9.45	9.6	0.372	0.388

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outlines(s) - Continued.

Device type	All	Device type	All	Device type	All	Device type	All
Case outlines	N	Case outlines	N	Case outlines	N	Case outlines	N
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CS1}$	19	I/O8	36	$\overline{CS4}$	53	I/O23
3	A5	20	I/O9	37	A17	54	I/O22
4	A4	21	I/O10	38	A18	55	I/O21
5	A3	22	I/O11	39	NC	56	I/O20
6	A2	23	I/O12	40	NC	57	I/O19
7	A1	24	I/O13	41	NC	58	I/O18
8	A0	25	I/O14	42	NC	59	I/O17
9	NC	26	I/O15	43	NC	60	I/O16
10	I/O0	27	V_{CC}	44	I/O31	61	V_{CC}
11	I/O1	28	A11	45	I/O30	62	A10
12	I/O2	29	A12	46	I/O29	63	A9
13	I/O3	30	A13	47	I/O28	64	A8
14	I/O4	31	A14	48	I/O27	65	A7
15	I/O5	32	A15	49	I/O26	66	A6
16	I/O6	33	A16	50	I/O25	67	$\overline{WE}$
17	I/O7	34	$\overline{CS2}$	51	I/O24	68	$\overline{CS3}$

FIGURE 2. Terminal connections.

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Power	Mode
V_{IH}	X	X	High Z	Standby	Standby
V_{IL}	V_{IL}	V_{IH}	High Z	Active	Read
V_{IL}	V_{IH}	V_{IH}	High Z	Active	Output disable
V_{IL}	X	V_{IL}	Data In	Active	Write

NOTES:

1. V_{IH} = High Logic Level
2. V_{IL} = Low Logic Level
3. X = Do no care (either high or low)
4. High Z = High Impedance State

FIGURE 3. Truth Table.

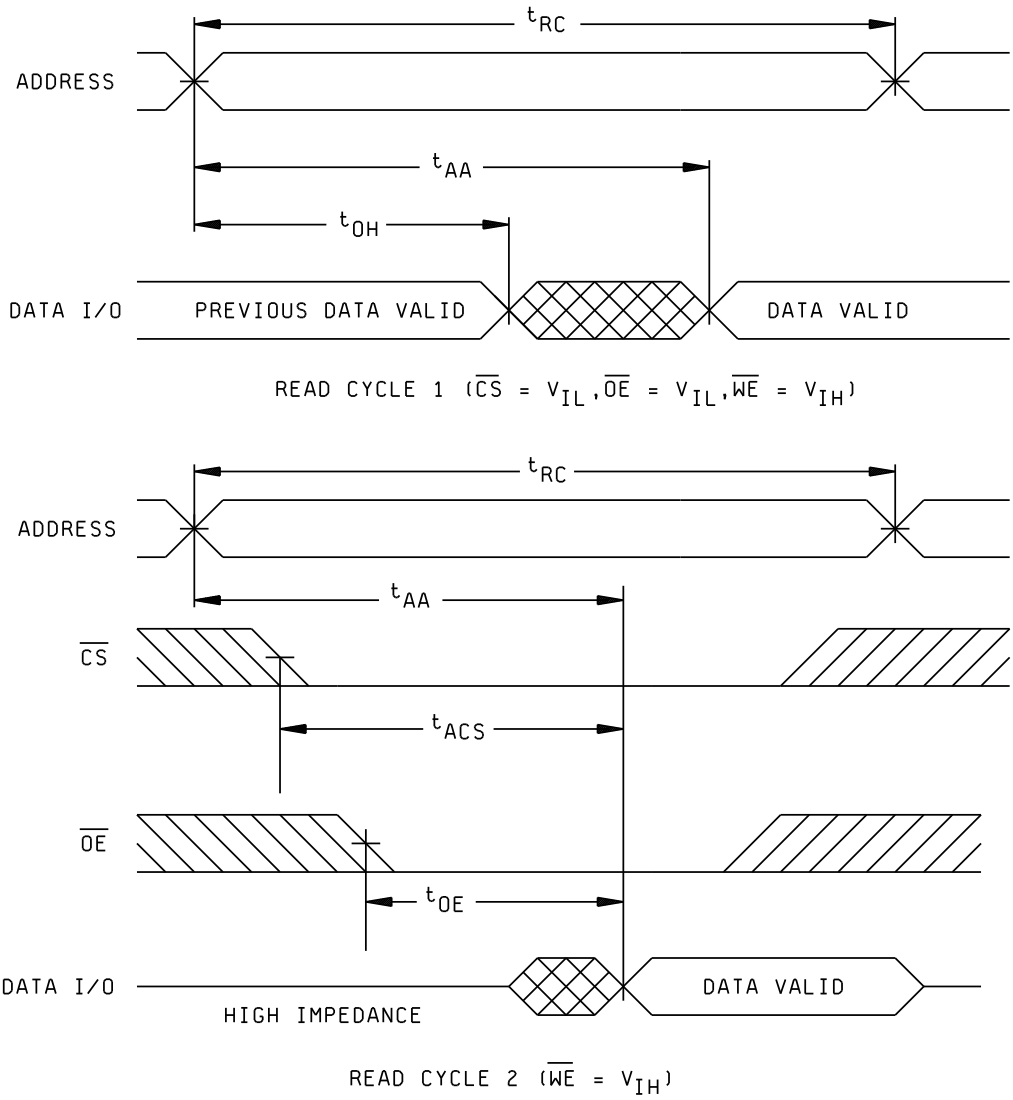
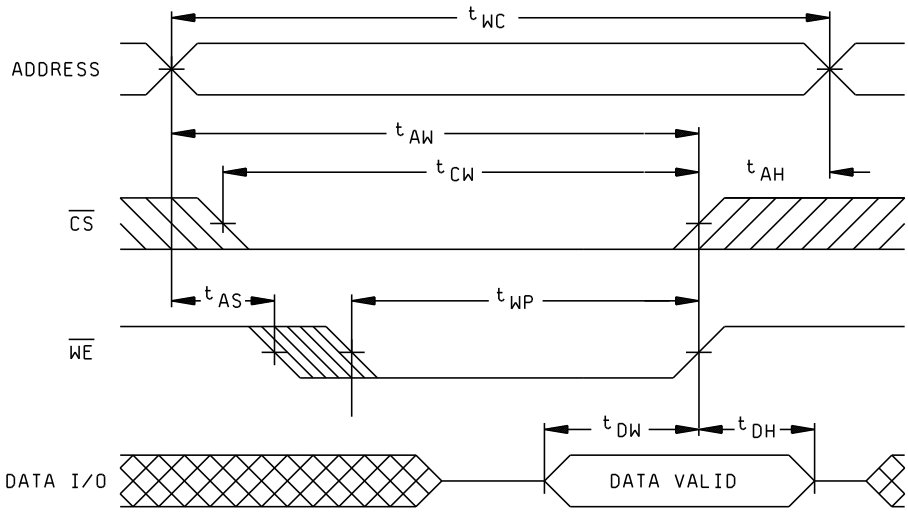
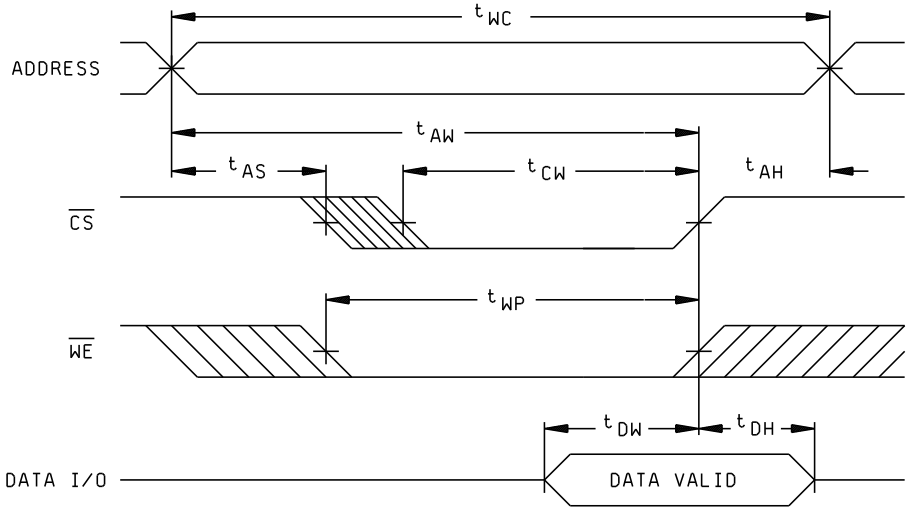


FIGURE 4. Read cycle timing diagram.



WRITE CYCLE 1 $\overline{WE}$ CONTROLLED



WRITE CYCLE 2 $\overline{CS}$ CONTROLLED

FIGURE 5. Write cycle timing diagrams.

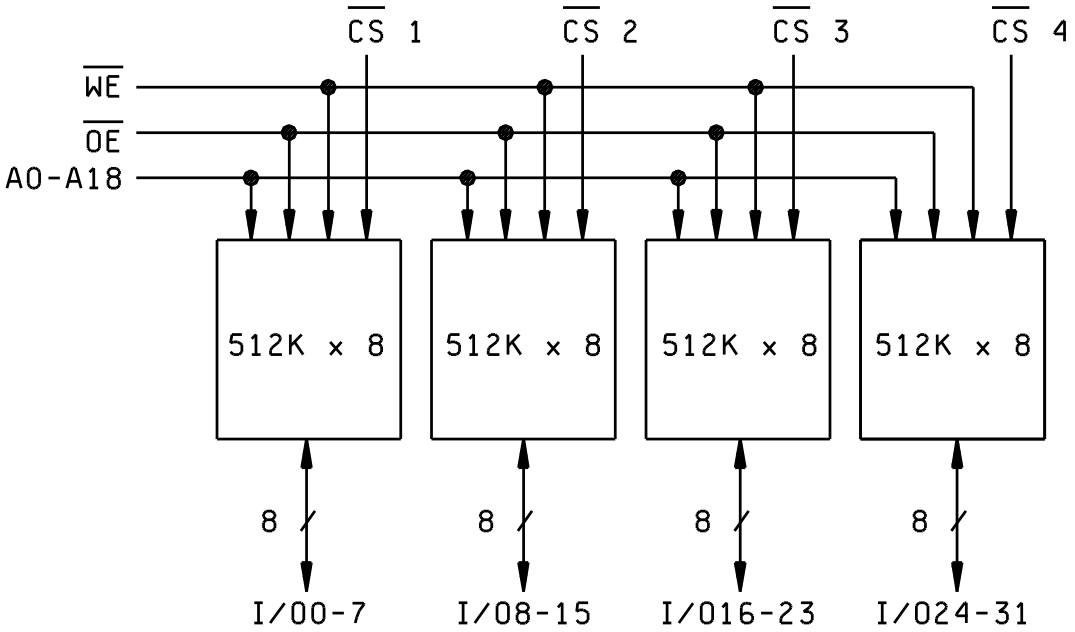
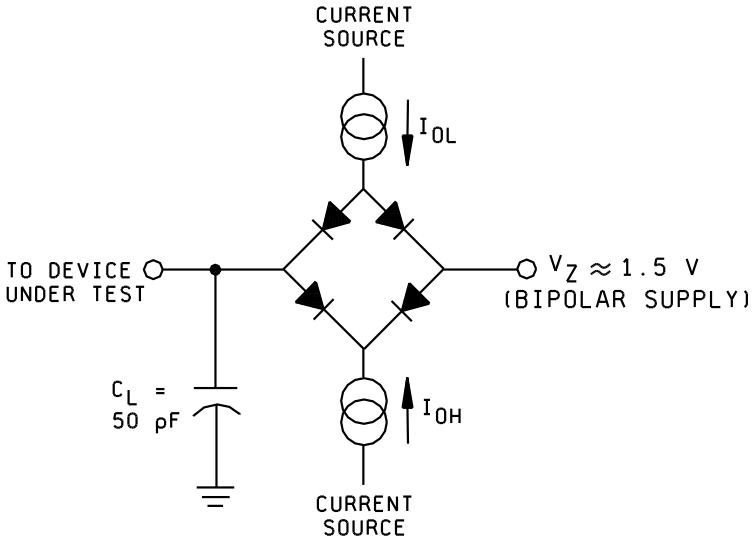


FIGURE 6. Block diagram.



Parameter	Typ.	Unit
Input Pulse Level	0 - 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Load Capacitance	50	pF

NOTES:
1. V_Z is programmable from +2 V to +7 V.
2. I_{OL} and I_{OH} are programmable from 0 to 16 mA.
3. Tester impedance is Z_0 = 75 ohms.
4. V_Z is typically the midpoint of V_{OL} and V_{OH}.
5. I_{OL} and I_{OH} are adjusted to simulate a typical resistive load circuit.
6. ATE tester includes jig capacitance.

FIGURE 7. Output load circuit.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534,group A test table)
Interim electrical parameters	1,4,7,9
Final electrical test parameters	1*,2,3,4,7,8A,8B,9,10,11
Group A test requirements	1,2,3,4,7,8A,8B,9,10,11
Group C end-point electrical parameters	1,2,3,4,7,8A,8B,9,10,11
MIL-STD-883, group E end-point electrical parameters for RHA devices	Subgroups ** (in accordance with method 5005, group A test table)

* PDA applies to subgroup 1.
** When applicable to this standard microcircuit drawing, the subgroups shall be defined.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534, and shall be conducted on all devices prior to conformance and periodic inspections. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table on firgure 3.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes H and K shall be M, D, R, and H. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for device classes H and K for levels M, D, R, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table II herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

d. For device classes H and K, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38534 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes H and K, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-7603.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0676.

6.6 Sources of supply for device classes H and K. Sources of supply for device classes H and K are listed in QML-38534. The vendors listed in QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 96-08-09

Approved sources of supply for SMD 5962-95624 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9562401HNC	54230	WS512K32F-120G4Q
5962-9562402HNC	54230	WS512K32F-100G4Q
5962-9562403HNC	54230	WS512K32F-85G4Q
5962-9562404HNC	54230	WS512K32F-70G4Q
5962-9562405HNC	54230	WS512K32F-55G4Q
5962-9562406HNC	54230	WS512K32F-45G4Q
5962-9562407HNC	54230	WS512K32F-35G4Q
5962-9562408HNC	54230	WS512K32F-25G4Q
5962-9562409HNC	54230	WS512K32F-20G4Q
5962-9562410HNC	54230	WS512K32M-45G4Q
5962-9562411HNC	54230	WS512K32M-35G4Q
5962-9562412HNC	54230	WS512K32M-25G4Q

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
54230	White Microelectronics 4246 East Wood Street Phoenix, Az 85040-1991